

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DKT. NO. 501.43228X00	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT MURATA, et al.			
		FILING DATE January 14, 2004		GROUP	

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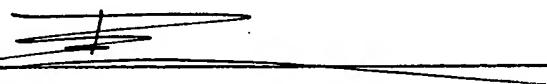
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
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							Yes	No
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PL	AU	WATANABE, et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995
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		07/05/05